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IN RE APPLICATION OF : Kesatoshi TAKEUCHI, et al.

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FOR: OVERLAY OF PLURAL IMAGES

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LETTER

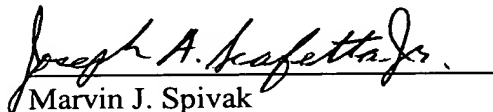
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Sir:

Submitted herewith is a partial English translation of reference JP 11-24641 for the Examiner's consideration. The reference cited therein has been filed on June 6, 2002.

Respectfully submitted,

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[0014] Fig. 2 illustrates the construction of a selector unit 30 applied in the first embodiment of the present invention. As shown in Fig. 2, 31A, 31B, 31C and 31D are selectors, which are controlled by the control signal, respectively. The selector 31A, 31B, 31C and 31D receive  
5 signals that are transmitted from buffers 22A, 22B, 22C and 22D, 22A and 22B, 22A, 22B, 22C and 22D, and 22A and 22D, respectively. At each selector, those received signals are controlled based on the control signal, as to whether of not each signal may go thorough.

[0015] In the following description, some applications for displaying the  
10 image corresponding to the resolution are shown with reference to the circuitry of Figs. 1 and 2. In one applicable example of displaying the image with high resolution requiring processing power of four image decoders, a parallel operation is performed on the image with all of image decoders 10A, 10B, 10C and 10D. As a result, the selector 31A and 31C  
15 on the selector unit 30 are configured to receive those image signals, however, the remaining selectors are configured not to let the signal through, for example, by the control signal that leads the flow of all image signals towards a main image scale conversion module 41A on a second image scale conversion unit 40 through the selector 31A.

[0016] In another applicable example of displaying the image data with  
20 high resolution requiring the processing power of two image decoders, the selector 31A is configured to switch over signals from buffers 22 A and 22 B, and the selector 31 C is configured to switch over signals from buffers 22 C and 22 D by the control signal that leads the flow of image  
25 signals towards the main image scale conversion module 41A or a sub image scale conversion module 41C. It depends on the size of the image to be displayed, based on the intension of the user, to decide the selector; the selector A or the selector C, where signals from the buffers 22A and 22B are passed.

[0017] In yet another applicable example of displaying the image data  
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with low resolution requiring the processing power of a single image decoder, image decoders 10A, 10B, 10C and 10D independently decode inputs of the image with image signals that are transmitted through buffers 22A, 22B, 22C and 22D, respectively, to the second image scale  
5 conversion unit 40, to which no processing is allocated or the display area specified by the user corresponds, via any one of the selectors; the selector 31A, 31B, 31C or 31D.

[0018] Thus, the image signal that has decoded the received image is converted into the image with the specific size at the image scale  
10 conversion modules 41A, 41B, 41C and 41D on the second image scale conversion unit 40, based on the user preference, and is integrally processed in the image overlay module 50 at the position corresponding to a couple of preset patterns, or at the position specified by the user arbitrary, in order to be output as one image.

15 [0019] In accordance with the first embodiment, the technique of the present invention enables the complicated image processing. In one example, one of two images with high resolution, which has been processed on image decoders 10A and 10B, is processed on the main image scale conversion 41A through the selector 31A. Two images with  
20 the standard resolution in the NTSC class (National Television System Committee color television), which has been decoded by image decoders 10C and 10D, are processed on sub image scale conversion modules 41C and 41D through selectors 31C and 31D, respectively. The resulting image in the former process and those two images are able  
25 to be output as one image with synchronous processing and the overlay processing. This application provides less load on the sub image scale conversion unit than the main image scale conversion unit, and thus deduces the size of the circuit.